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				Application Number	10/718,920
				Filing Date	11/21/2003
				First Named Inventor	Chi, et al.
				Art Unit	TBD
				Examiner Name	TBD
				Attorney Docket Number	TSM03-0422
Sheet	1	of	2		

[illegible][illegible]

Examiner Signature	<i>Andrew K...</i>	Date Considered	03/30/05
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Substitute for form 1449B/PTO		Complete if Known			
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	10/718,920		
		Filing Date	11/21/2003		
		First Named Inventor	Chi, et al.		
		Art Unit	TBD		
		Examiner Name	TBD		
Sheet	2	of	2	Attorney Docket Number	TSM03-0422

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
ah	2	Rim, K., et al., "Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's," IEEE Transactions on Electron Devices, vol. 47, no. 7, pp. 1406-1415, July 2000.	
ah	3	Rim, K., "Strained Si Surface Channel MOSFETS for High-Performance CMOS Technology," IEEE International Solid-State Circuits Conference, paper #7.3, pp. 116-117, 2001.	
ah	4	Yeo, Y.C., et al., "Enhanced performance in Sub-100 nm CMOSFETs using Strained Epitaxial Silicon-Germanium," International Electron Device Meetings, pp. 753-756, 2000.	
ah	5	Ootsuka, F., et al., "A Highly Dense, High-Performance 130nm Node CMOS Technology for Large Scale System-on-a-Chip Applications," International Electron Device Meetings, pp. 575-578, 2000.	
ah	6	Ito, S., et al., "Mechanical Stress Effect of Etch-Stop Nitride and Its Impact on Deep Submicron Transistor Design," International Electron Device Meetings, pp. 247-250, 2000.	
ah	7	Shimizu, A., et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," International Electron Device Meetings, pp. 433-436, 2001.	
ah	8	Ola, K., et al., "Novel Locally Strained Channel Technique for High Performance 55nm CMOS," International Electron Device Meetings, pp. 27-30, 2002.	
ah	9	Scott, G., et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress," International Electron Device Meetings, pp. 827-830, 1999.	
ah	10	Bianchi, R.A., et al., "Accurate Modeling of Trench Isolation Induced Mechanical Stress Effects on MOSFET Electrical Performance," International Electron Device Meetings, pp. 117-120, 2002.	

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